

PATENT ABSTRACTS OF JAPAN

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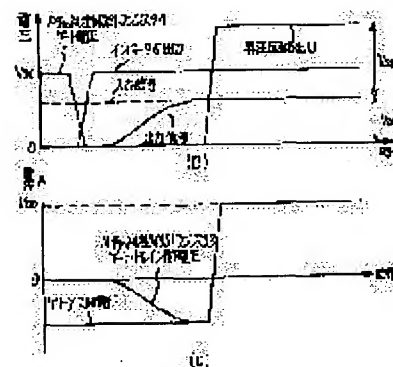
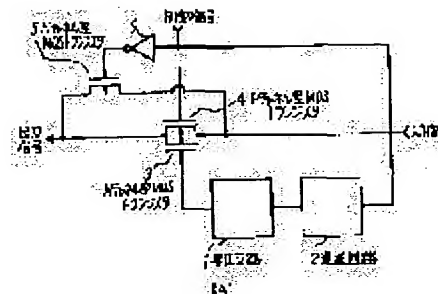
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(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PURPOSE: To realize an analog switch workable in a range of a power supply voltage of nearly 5V from a low power supply voltage (threshold level $V_{TP} + V_{TN}$) of a mutually complementary transfer gate.

CONSTITUTION: An N-channel MOS transistor (TR) 5 is connected in parallel between an input and output of a complementary transfer gate comprising an N-channel MOS TR 3 whose source is used for an input terminal and whose drain is used for an output terminal and a P-channel MOS TR 4. Then a control signal is given to a gate of the TR 3 via a delay circuit 2 and a boosting circuit 1, a gate of the TR 5 via an inverter 6 and a gate of the TR 4 respectively.



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